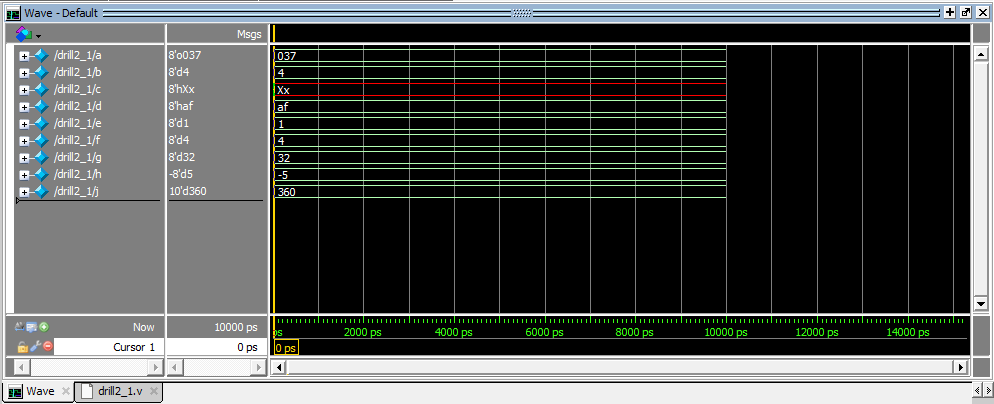
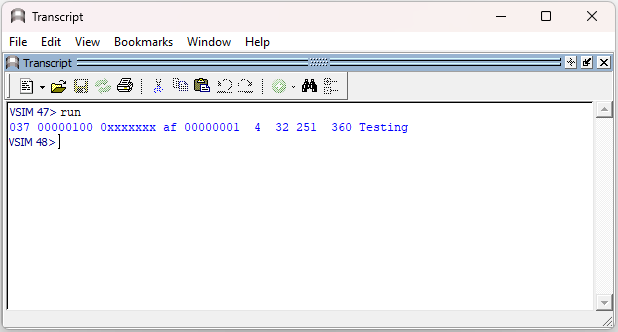
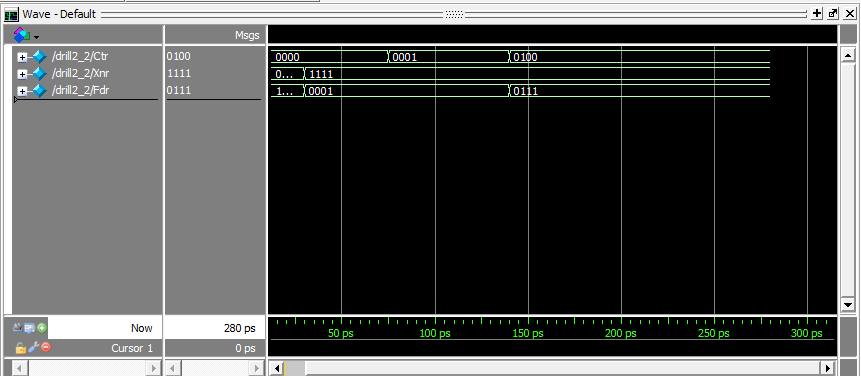
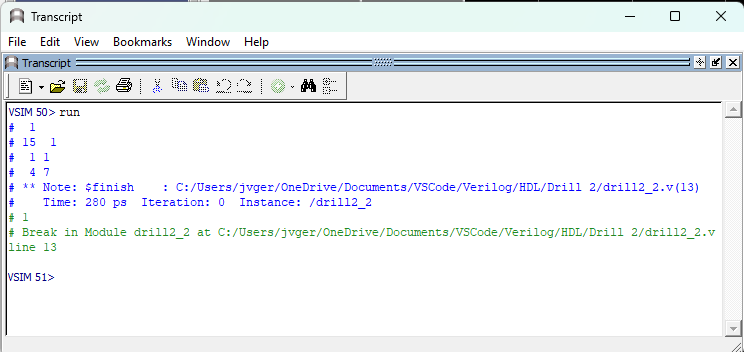
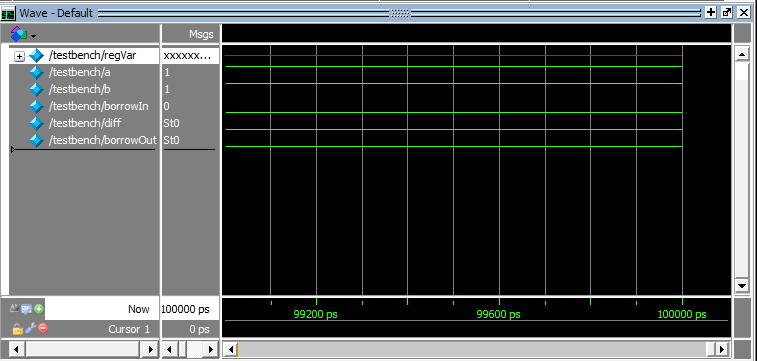
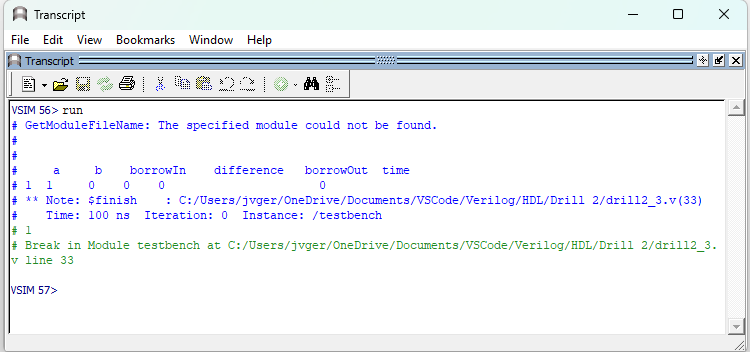
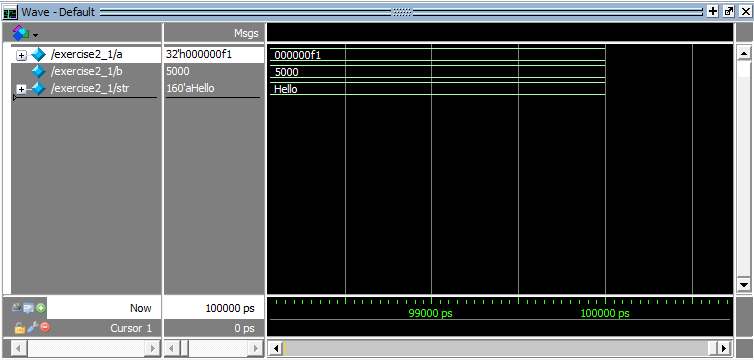
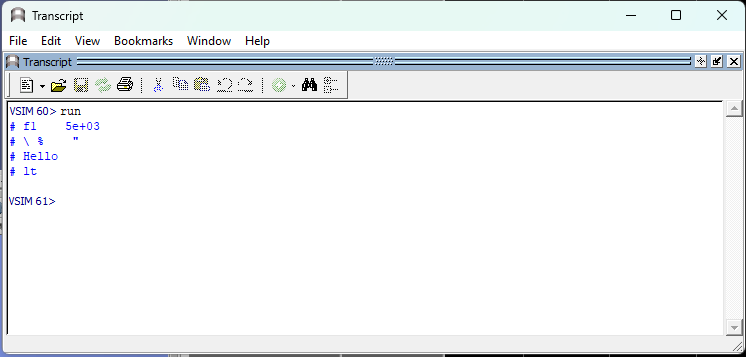
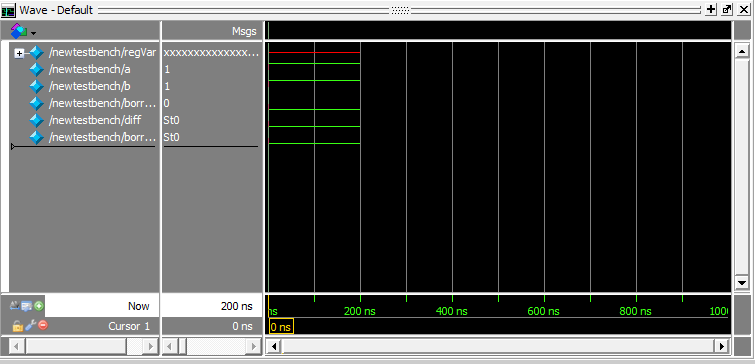
DRILL 2

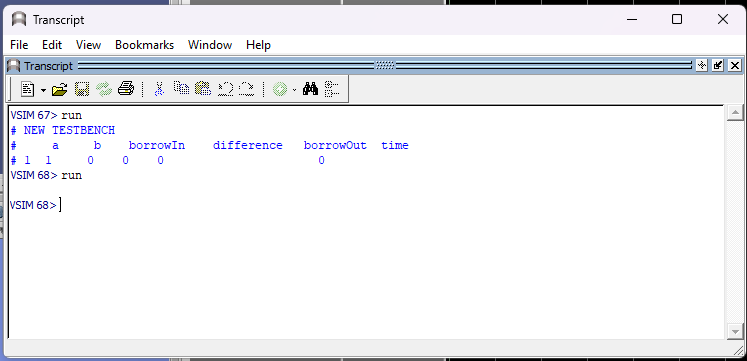
* **Drill2\_1.v**
  + Testbench
  + Transcript
* **Drill2\_2.v**
  + Testbench
  + Transcript
* **Drill2\_3.v**
  + Testbench
  + Transcript

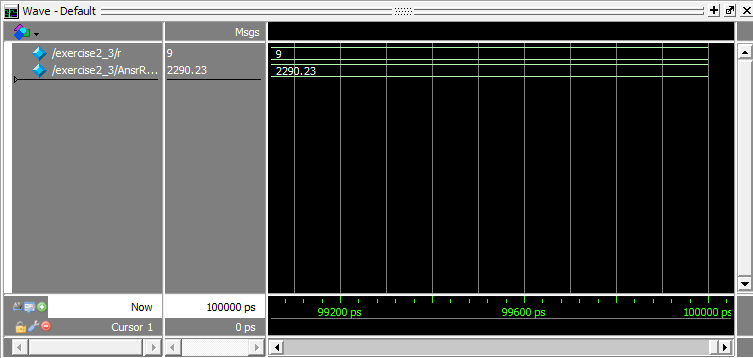
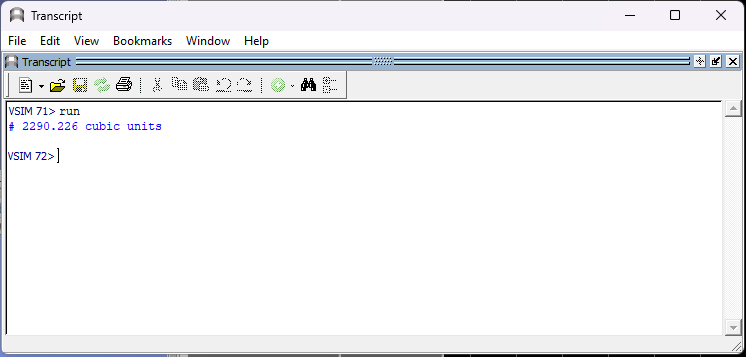


* **Exercise2\_1.v**
  + Testbench
  + Transcript
* **Exercise2\_2.v**
  + Testbench



* + Transcript



* **Exercise2\_3.v**
  + Testbench
  + Transcript

**Review Questions**

1. **What is the difference between vectors X [5:0] and X [0:5]?**

*The difference between vectors X [5:0] and X [0:5] is that the vector X [5:0] specifies the six least significant bits (LSB) of X, while the vector X [0:5] specifies the six most significant bits (MSB) of X.*

1. **How are negative numbers represented? How does Verilog treat these numbers?**

*To represent a negative number in Verilog, the 2's complement is used, despite the convention of using a minus or negative sign before the size for a constant number. This involves inverting the bits of the number and adding 1 to the result.*

1. **What happens in integer numbers if the size is greater than the value? What if the size is less than the value?**

*When the size is greater than the value, the leftmost bits will be padded with zeroes. On the other hand, if the size is less than the value, any overflowed bits in the leftmost position will be ignored or disregarded.*

1. **When are white spaces significant in your programs?**

*White spaces in Verilog can include characters for tabs, newlines, and form feeds, in addition to spaces. These white spaces play a crucial role in separating tokens, making it important to use them as token separators.*

1. **Evaluate the following:**

*A=8’b10101010 B=8’b01101110 C=8’b11101011*

|  |  |
| --- | --- |
| *B&C* | ***8'b01101010*** |
| *|A* | ***1*** |
| *~^C* | ***1*** |
| *A||B* | ***1*** |
| *A>C* | ***0*** |
| *B<=A* | ***1*** |
| *C<<2* | ***8'b10101100*** |
| *B\*2* | ***8'b11011100*** |
| *C%A* | ***8'b01000001*** |
| *A-B* | ***8'b00111100*** |

1. **When is x (unknown or don’t care) assigned during simulation, and when does high impedance z occurs?**

*In HDL, the value for "Unknown" or "don't care" is assigned as "x" during variable declaration. On the other hand, "High impedance" or "z" occurs when the signal is neither at logic high (1) nor logic low (0). This indicates that the signal is not connected to anything, which is referred to as "floating" in hardware or circuits.*